

Crystalline Silicon Solar Cells With Two Different Metals

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Abstract. We report crystalline silicon solar cells with two different metals, Thermally grown SiO₂ 1.5~2-nm thick passivated the surfaces of n-type silicon substrates. Inter digit stripes of Al and Au with a width of 500 μm and a gap of 100 μm were formed on the top surface in order to cause an asymmetric internal built-in potential distribution in silicon because of the difference between their work functions of 0.92 eV. Solar cell characteristics were observed by halogen lamp illumination at 22 mW/cm². The short-circuit current density and open-circuit voltage were 14.7 mA/cm², 0.47 V. The conversion efficiency was estimated to be 15.5%.

Introduction

Semiconductor solar cells have been attractive as a device for producing electrical power from sunlight [1]. The conversion efficiency and production cost are essential points in the advancement of the solar cell industry and its business. Many important technologies have been developed to improve those points, such as shallow PN junction formation, back-surface field formation, defect passivation, and multijunction formation [2,3]. Simple processing is still attractive for the low-cost fabrication of solar cells.

In this paper, we report a simple silicon solar cell with two different kinds of metals [4]. This solar cell does not need the PN junction, transparent electrode for light correction, and silver printed electrode for current correction. We discuss the physics of the solar cell and its technical possibilities. We then report current voltage characteristics of the solar cells.

Physics

Figure 1 shows distribution of the work function of different metals reported by H. B. Michaelson [5]. The work function widely ranges from 2 to 6 eV. Alkaline and alkaline earth metals have low work functions. It is well known that gold (Au), platinum, and nickel have high work functions. Silicon can have a work function ranging from 4.1 to 5.2 eV, which depends on impurity doping, as shown in Fig. 1. Figure 2 shows a schematic

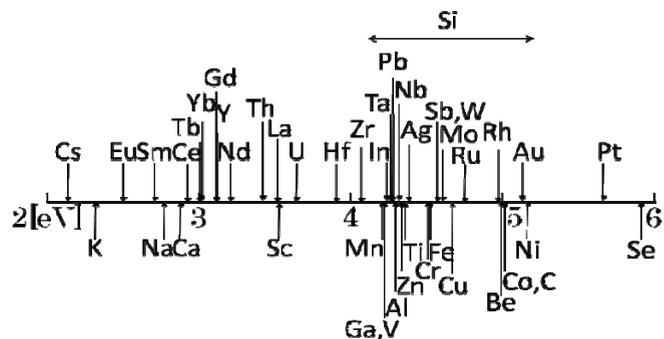


Fig. 1. Distribution of work functions for different kinds of metals as well as crystalline silicon.

image of the energy band structure when n-type crystalline silicon is sandwiched by Al and Au metals via thin SiO₂ layers zero-biased at the both metals. Their work functions of Al and Au are reported as 4.18 and 5.1 eV, respectively [5]. The difference in the work functions of those metals can cause an asymmetric distribution of the internal built-in potential in silicon. Because the initial Fermi level of n-type silicon is near the work function of Al, but far different from that of Au, a large internal potential distribution associated with the depletion region is spatially formed near the Au metal electrode, as shown in Fig. 2. SiO₂ layers have an important role of stable

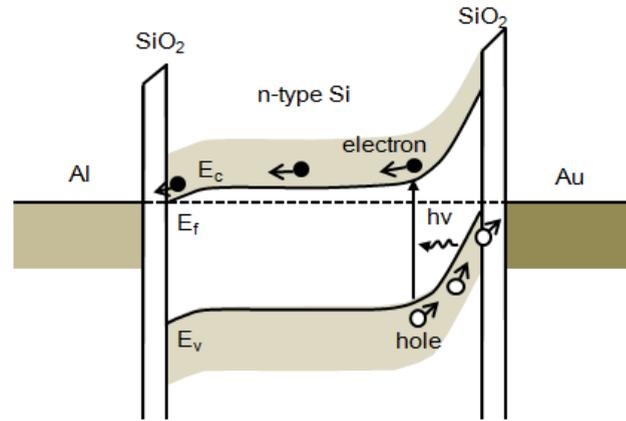


Fig. 2. Schematic energy band image of present solar cell for n-type silicon with Al and Au electrodes.

passivation of silicon surface with a low density of interface traps and a low recombination velocity of the minority carriers in order to maintain the asymmetric distribution of the internal built-in potential. Holes and electrons excited by light illumination in silicon separate each other according to the internal potential distribution, as shown in Fig. 2. Holes move toward the Au electrode, and electrons move toward the Al electrodes. The SiO₂ layers should be thin and electrically conductive associated with the quantum-tunneling effect to produce photo-induced current from silicon to the two metals [6, 7]. Although 1.2 nm thermally grown SiO₂ has been already in production stage in the very large scale integrated circuit technology field, the substantial tunneling leakage characteristic has blocked its application to metal-oxide semiconductor field effect transistor. On the other hand, the thin SiO₂/Si interface with the tunneling conductive characteristic will be suitable for our solar cell model.

Figure 3 an overview image of a practical cell structure for our solar cells. The both silicon surface are passivated with SiO₂ layers to keep the minority carrier lifetime (τ_{eff}) high. Top SiO₂ was thin enough for the tunneling current effect. Al and Au inter digit patterns are formed on the top surface. The band structure shown in Fig. 2 is completed along Al, top SiO₂, silicon (lateral direction), top SiO₂, and Au. Light is illuminated to the rear surface. Holes and electrons generated at the rear surface travel to the top surface. Holes and electrons come into Au and Al electrodes, respectively. The solar cell does not need the PN junction, transparent electrodes and Ag printed electrodes, as shown in Fig. 3. This is a clear advantage for reduction of fabrication cost of solar cell. In addition, no doped layer would result in a low Auger recombination probability, which would lead a high conversion efficient [8,9]. In order to

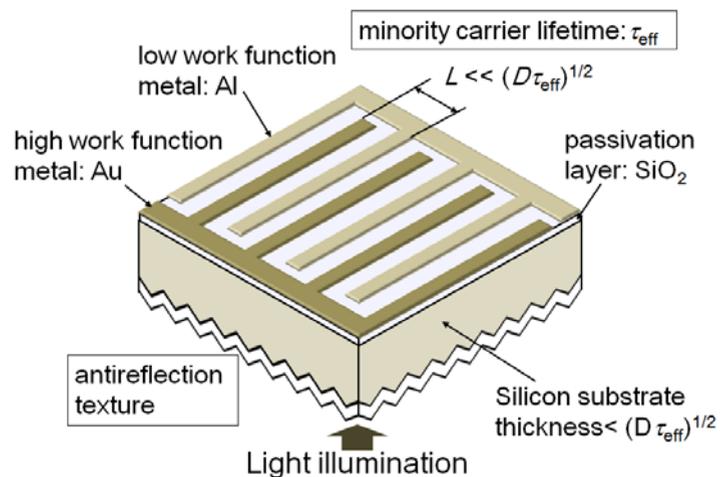


Fig.3 Overview image of a practical cell structure for our solar cells

achieve a high efficiency cell, as shown by the structure in Fig. 3, thin and good passivation of silicon surfaces is essentially important. Moreover, metal electrodes should be patterned densely with widths and gaps smaller than the minority carrier diffusion length $(D\tau_{\text{eff}})^{0.5}$ for effectively collecting photo-induced carriers. The substrate thickness should be also thinner than $(D\tau_{\text{eff}})^{0.5}$ for effective carrier diffusion from the rear surface to the top surface. Anti-reflection surface texture will be necessary at the rear surface for effective light collection.

Experimental demonstration

N-type single-crystalline silicon substrates with a thickness of 520 μm and a resistivity of 30 Ωcm were used. The mirror-polished top and rear surface were thermally oxidized, and 100-nm-thick thermally grown SiO_2 layers were formed on both surfaces. The SiO_2 layer at the top surface was then thinned with buffered hydrofluoric acid. The thickness of SiO_2 was estimated to be 1.5~2.0 nm by analyzing the optical reflectivity spectra [10]. Samples were then annealed at 260°C for 3 h in 1.3×10^6 Pa H_2O vapor to further passivate the silicon surface [11]. On the top surface, Al and Au inter digit patterns are formed with their width of 500 μm , length of 1 cm, and a gap of 100 μm . Light illumination was conducted to the rear surface using halogen lamp at 22 mW/cm^2 . Light illumination area was defined to be 1 cm^2 using a window mask. Light reflection loss about 20% probably occurred because no anti-reflection structure was formed at the rear surface.

The minority carrier effective lifetime, τ_{eff} , was measured by 9.35 GHz microwave transmission measurement [12]. τ_{eff} was 1200 μs for the initial silicon substrates with both surfaces coated with 100-nm-thick SiO_2 layers. The silicon surfaces were well passivated by the SiO_2 layers. When the thickness of SiO_2 films at the top surface was decreased to 1.5~2.0 nm using buffered hydrofluoric acid, τ_{eff} markedly decreased to 7.6 μs . This means that the carrier recombination rate at the top surface was increased after SiO_2 etching. The subsequent 1.3×10^6 Pa H_2O vapor heat treatment at 260°C for 3 h increased τ_{eff} to 54 μs . Surface passivation was improved by the high-pressure H_2O heat treatment and τ_{eff} increased. The minority carrier diffusion length, $(D\tau_{\text{eff}})^{0.5}$ was estimated to be about 250 μm using a diffusion coefficient of 12 cm^2/Vs for hole. The width of Al and Au electrodes and substrate thickness were larger than that minority carrier diffusion length. Therefore, some degree of carrier annihilation probably occurred via carrier recombination during carrier diffusion.

Figure 4 shows the absolute electrical current density as a function of voltage for samples with Al and Au stripes in the dark and illuminated with light to the rear surfaces. The electrical current density was obtained from experimentally electrical current divided by an electrode area of 0.44 cm^2 in the case of dark. On the other hand it was obtained from experimentally electrical current divided by the illumination area of 1 cm^2 in the case of light illumination. The electrical current increased as the positive voltage increased under the dark condition. Typical metal-insulator semiconductor diode characteristic was observed. It means that hole density at SiO_2/Si interface below Au

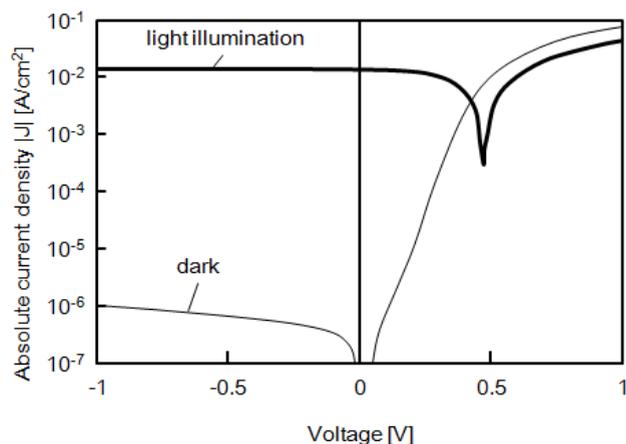


Fig. 4 Absolute electrical current as a function of applied voltage.

electrode was sensitively increased by positive gate voltage application. Substantial tunneling current via the top thin SiO₂ layer was observed. Light illumination markedly increased the electrical current density. It indicates that photo-induced holes and electrons were generated at the rear surface and traveled across the 520- μm -thick silicon substrate to the top surface and flowed into Au and Al, respectively, in accordance with the internal built-in potential. No current appeared at 0.47 V, indicating an open-circuit voltage. Typical solar cell current voltage characteristics were obtained as shown in Fig. 5. In the case of light illumination to the rear surface, the short-circuit current density J_{sc} , and the open-circuit voltage V_{oc} were 14.7 mA/cm², 0.47 V, respectively. The conversion efficiency was estimated to be 15.5 %.

Those results shown in Figs. 4 and 5 demonstrate our simple solar cell model. However, the present fabrication process was not yet optimized. The series resistivity was estimated to be about 9 Ωcm^2 from the minimum differential resistivity of the solar cell characteristic around V_{oc} shown in Fig. 5. The V_{oc} of 0.47 V was lower than we expected from the difference in the work functions of Al and Au of 0.92eV. We believe that those problem is overcome by improvement in surface passivation. Process technologies for formation of thin and good SiO₂ layers should be improved to achieve a high tunneling effect, a low density of interface trap states and low recombination velocity.

Moreover, the width of electrodes should be small less than effective carrier diffusion length. The substrate thickness should be also thin less than effective carrier diffusion length.

For our solar cell model, it is essential that the difference in the work functions of two different kinds of metals causes an internal built-in potential in the semiconductor. Many other choices of metals will be possible besides the Al-Au pair used in the present work. For example, H_f and Au have a large difference of 1.2 eV in the work function [5]. This has the advantage of causing a high internal built-in potential in silicon. The present model may be applied to many other semiconductors if two different metals with appropriate work functions are selected.

Summary

Crystalline silicon solar cells were demonstrated. N-type 520- μm -thick 30 Ωcm single-crystalline silicon substrates coated with 100-nm-thick thermally grown SiO₂ layer at the top surface was thinned to 1.5~2.0 nm using buffered hydrofluoric acid. Samples were then annealed at 260°C for 3h in 1.3x10⁶ Pa H₂O vapor. The minority carrier effective lifetime was 54 μs . Inter digit stripes of Al and Au with a width of 500 μm and a gap of 100 μm on the top surface. Electrical current as a function of voltage was measured between Al and Au stripes under light illumination of a halogen lamp at 22 mW/cm² to the rear surface. Typical current voltage characteristics of solar cells were obtained. J_{sc} and V_{oc} were 14.7 mA/cm² and 0.47 V, respectively. The conversion efficiency was 15.5%. Holes and electrons generated at the rear surface traveled across the 520- μm -thick silicon substrate and flowed into Al and Au electrodes, respectively, owing to a tunneling effect. Those results demonstrated our solar cell physics that

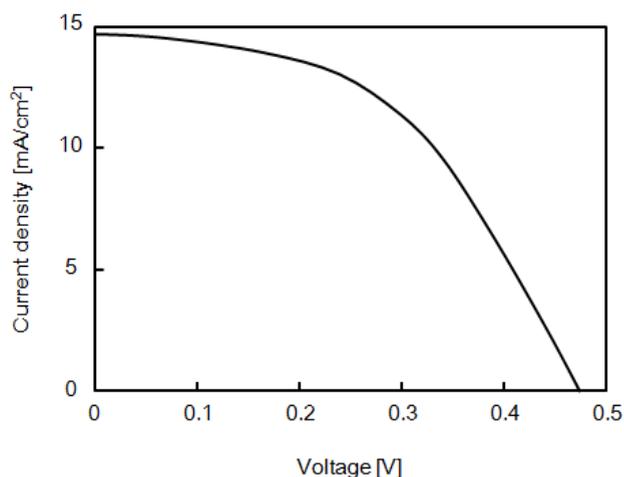


Fig. 5 Solar cell characteristics for light illumination to the rear surfaces.

a difference in the work functions of two different kinds of metals causes an internal built-in potential in silicon.

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