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Electrical properties of thin film transistors with ZnO channel layer deposited by atomic layer deposition

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Abstract. We investigated zinc oxide (ZnO) thin films by atomic layer deposition (ALD) for the application of thin film transistors (TFTs). The fabricated TFTs were annealed at various temperatures, in an oxygen ambient gas. Annealing at the temperature up to 400 ℃ improved the characteristics of TFTs without any degradation of the subthreshold swing or any large shift of the threshold voltage. From the annealing temperature dependence of transfer characteristics and x-ray diffraction patterns, we found that the improvement of electrical characteristics is attributable to the crystalline modification of ZnO films. The TFTs annealed at 400 ℃ in the O_2 ambient improved the stability for the bias stress. Secondary ion mass spectrometry measurements revealed marked decrease of hydrogen in the ZnO channel layer after the annealing at 400 ℃.

Introduction

Amorphous (a-Si:H) and polycrystalline silicon (poly-Si) have been widely used for an active channel layer in thin film transistors (TFTs). However, there are a number of drawbacks in these materials, such as the high temperature fabrication process and their limited performance. In recent years, the application of zinc oxide (ZnO) thin films as an active channel layer in TFTs has become of great interest owing to its specific characteristics. [1-3] ZnO is transparent to visible wavelengths because of the wide band gap (~3.37 eV), and the availability of high-quality ZnO films over large areas at low temperature suggests compatibility with plastic or flexible substrates. It has recently been demonstrated that the field effect mobility of ZnO TFTs is higher than that of a-Si:H TFTs. To take advantage of the high performance of ZnO, the issue of stability should be solved.

To ensure the stability of ZnO thin films, we focused on an atomic layer deposition (ALD) method. The ALD method is one of the thin film preparation techniques, which is widely studied in LSI industry. The ALD thin film is deposited with alternating exposures of a source gas and an oxidant. The ALD film has features of accurate thickness control, high conformity, and uniformity over large areas, because of the layer-by-layer growth. [4] It is reported that the TFTs with ALD ZnO channel layers demonstrated high mobility. [5 - 7]

In this study, we fabricated TFTs using ZnO thin film as the channel layer deposited by ALD, and investigated the stability. The dependence of TFT characteristics on the annealing condition is evaluated, and the reliability of TFTs is characterized by applying the bias stress.

Experimental

The schematic structure of bottom-gate type ZnO TFTs fabricated in this study is shown in Fig.1. 50-nm-thick SiO_2 gate insulator was prepared by a thermal oxidation method. 30-nm-thick ZnO thin films were deposited on p-type Si (100) substrates by plasma assisted ALD (PA-ALD) using alkyl-Zn as a metal precursor and oxygen radical (O*) as a reactant at the substrate temperature of 100 ℃. Ti metal was deposited and patterned by lift-off technique for the source/drain (S/D) electrodes. The Si substrate was used as the gate electrode.

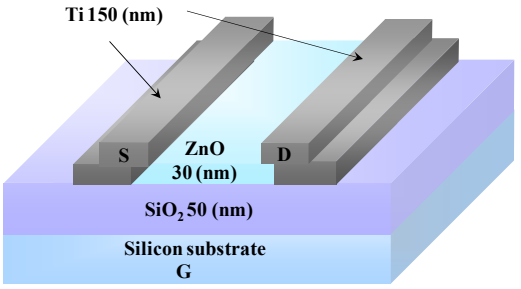

Fig.1. Bottom-gate ZnO TFT

The fabricated TFTs were annealed at 100 ~500 ℃ for 1hour in an O_2 (O_2 =20 %, N_2=80 %) ambient. [8] The electrical properties were measured using a semiconductor parameter analyser (Agilent 4156C).

The channel length (L) and width (W) used in this study were 10 and 20 μm, respectively. The threshold voltage (V_{th}) was defined by the gate voltage (V_g), which induces a drain current of 1 nA at a drain voltage (V_d) of 5 V. The on/off current ratio was measured by the ratio of maximum to minimum drain current (I_d) on the gate voltage axis, and on-current (I_{d_on}) was defined as the drain current measured with V_g = 10 V.

Results and Discussion

Electrical characteristics: Transfer characteristics of TFTs annealed at various temperatures in O_2 ambient were measured in a single-sweep mode of the gate voltage with V_d = 5 V. The variation of the transfer characteristics and the I_{d_on} as a function of the O_2 annealing temperature are shown in Figs. 2(a) and 2(b), respectively. For the ZnO TFTs annealed at 350 ℃ in O_2 ambient, the off-current (I_{d_off}) was 2.0×10^{-14} A, and the on/off ratio was 5×10^{9}. The field effect mobility was about 2.1 cm^2/Vs, the V_{th} was -2.1 V, and the subthreshold swing (*S.S.*) was 0.22 V/decade. The TFTs annealed over 450 ℃ showed lower I_{d_on} than that annealed at 400 ℃. We suppose that the deduction of the I_{d_on} of TFTs annealed over 450 ℃ are due to the oxidation of Ti used for S/D electrodes.

From the measurement of electrical properties in the fabricated TFTs annealed in O_2 ambient, it is assumed that the oxygen deficiencies were reduced by the introduction of oxygen during the annealing, resulting in the clear transistor operation.

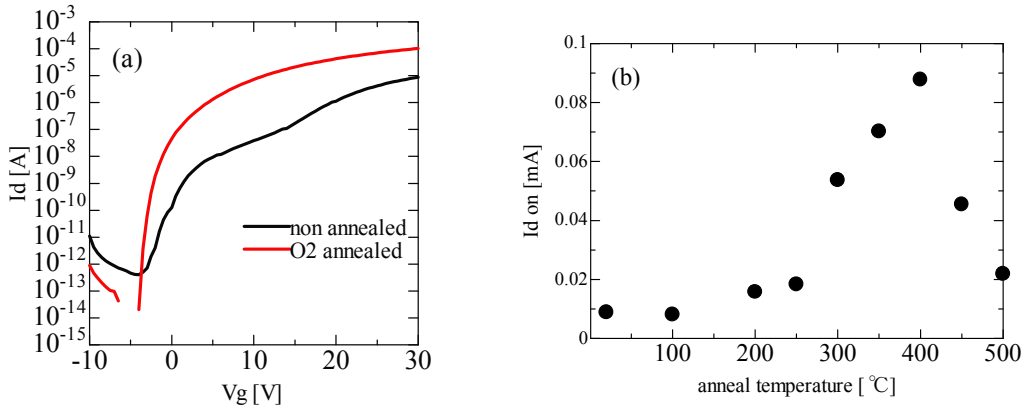

Fig.2. (a) I_d-V_g characteristics non-annealed and annealed at 350℃, O_2 ambient. (b) I_{d_on} of ZnO-TFTs annealed at O_2 ambient as a function of annealing temperature. (V_d=5 V)

XRD measurement: Crystal structure of the ZnO films was characterized by x-ray diffraction (XRD) measurements. Figures 3(a) and 3(b) show x-ray diffraction patterns of ZnO films used for the fabrication of the ZnO TFTs. In Fig.3 (a), three dominant peaks were observed from the as-deposited and 300 ℃-annealed ZnO films, which originate from the (100), (002), and (101) reflections. In Fig.3 (b), (002) diffraction peaks of as-deposited and 200 ~400 ℃ -annealed ZnO films are shown. The (002) peak positions of the 2θ scans, and the lattice constant c calculated from the peak positions are summarized in Tab. I. In the films annealed at 300 ~400 ℃, the intensity of (002) peaks was slightly higher than that of (100) peaks. The resistivity of ZnO films is affected by the number of grain boundaries and the phase at grain boundary. [9 -11] These results suggest that the resistivity is reduced by the (002) preferred orientation of the film annealed over 300 °C. Further, (002) peak shifted to a high angle of 2θ of the ZnO films annealed above 200 °C, and thus the lattice constant c of the ZnO films was reduced. This reduction of the lattice constant toward the characteristic value of ZnO by annealing implies release of the strain of the ZnO films. It can be estimated that the strain of grains in non-annealed film was considerably improved by the annealing. These changes are well matched with the increasing of I_{d_on} by annealing. Compared with the temperature dependence of electrical properties, the changes of the transfer characteristics by annealing are possibly related to the reduction of the lattice constant.

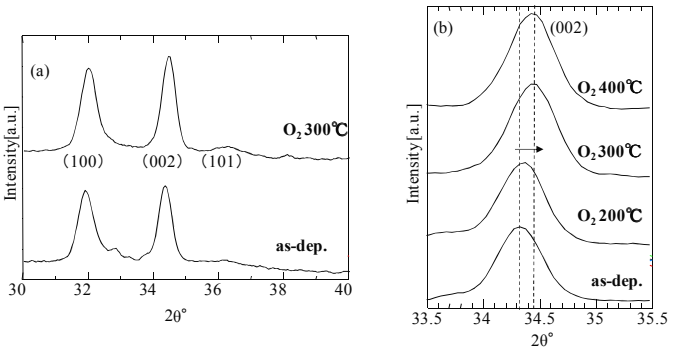

Fig.3. (a) XRD patterns of ZnO films annealed at 300℃. (b) Dependence of (002) peaks of ZnO films on the annealing temperature.

Table I. Results of XRD measurement

	Non-anneal	O_2 , 300℃	characteristic value[2)]
2θ° at (002) peak of ZnO film	34.325	34.425	34.422
Lattice constant c[Å]	5.221	5.206	5.204

Bias stress stability: The stability of TFTs under bias stresses is of crucial importance for their application to display driver. [12, 13] To evaluate the device stability, we measured the variation of the transfer characteristics under gate and drain bias stresses at room temperature. The stressing condition was 20 V of the V_g with 20 V of the V_d. The stress was applied for various periods of time up to 10000 s.

Figures 4(a) and 4(b) show the transfer characteristics before and after stressing periods of 1, 10, 100, 1000 and 10000 s. Figure 4 (a) shows bias stress stability of the TFTs

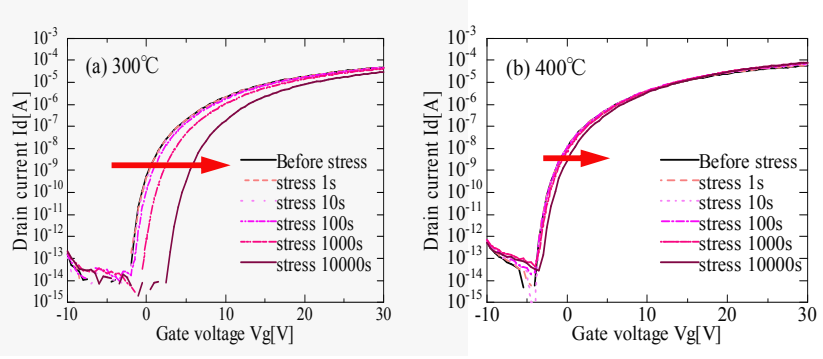

Fig. 4. Transfer characteristics of ZnO TFTs annealed at (a) 300℃, and (b) 400℃ under the stress (V_g =20 V, V_d = 20 V)

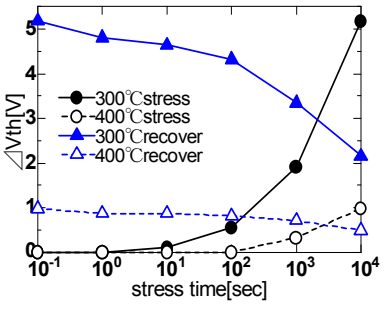

Fig.5. The ΔV_{th} during stressing (V_g=20 V, V_d=20 V), and recovery.

annealed at 300 °C in O_2 ambient, and Fig. 4 (b) shows that annealed at 400 °C. The positive shift of the V_{th} (~ +5.2 V) was observed after 10000seconds stressing in the TFTs annealed at 300 °C, while the V_{th} shift was remarkably reduced in the TFTs annealed at 400 °C. After the imposition of the stress, the transfer characteristics were measured in the absence of the stress at room temperature. Immediately after turning off the stress, the ΔV_{th} was recovered gradually as time advances as shown in Fig.5. For a recovery time of 10000 s, transfer characteristics almost recovered to the initial state. This behavior was not observed in poly-Si or a-Si:H TFTs, for which thermal annealing was required for these TFTs to recover. [14] The variation of the subthreshold swing (ΔS) was not varied with the stress time.

Figures 6 (a) and 6 (b) show the changes in the transfer characteristics of ZnO TFTs annealed at 300 and 400 ℃ under the gate voltage stress of V_g = 20 V. Since the V_d was 0 V, an uniform and transverse electric field was formed across the channel. Similar ΔV_{th} and no variation of *S.S.* were observed between with and without drain bias stress applied. Furthermore, for the drain voltage stress with no gate voltage bias, no marked degradation was observed.

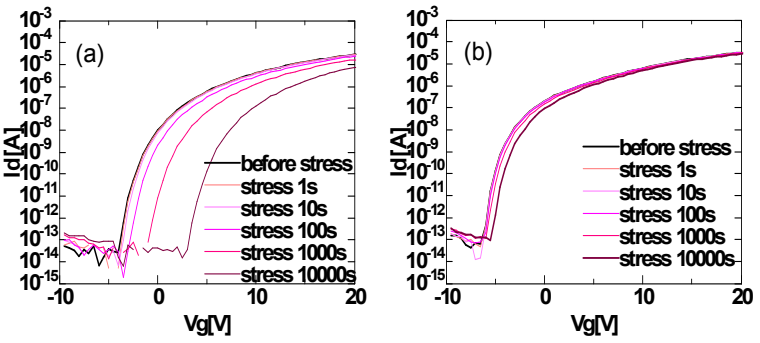

Fig.6. Transfer characteristics of ZnO TFTs annealed at (a) 300℃, and (b) 400℃ under the stress (V_g =20 V, V_d = 0 V)

These results suggest that ΔV_{th} is exclusively attributed to the gate bias stress. It was reported that there are two prominent mechanisms of ΔV_{th} in a-Si:H TFTs under positive gate voltage stresses. The ΔV_{th} caused by the state creation process shows power law time dependence, while the ΔV_{th} caused by the charge trapping process shows a logarithmic time dependence. [15 -17] This suggests that these V_{th} shifts in ZnO TFTs under stress are due to charge trapping near the interface between ZnO channel layer and SiO_2 gate insulator.

SIMS measurement: Secondary ion mass spectrometry (SIMS) measurements were performed for ZnO films non-annealed, and annealed in O_2 ambient at 200 ℃, 300 ℃ and 400 ℃ as shown in Figs.7 (a), (b), (c), and (d), respectively. Further, fig. 8 shows the dependence of hydrogen in ZnO films and ΔV_{th} after 10000seconds stressing on annealing

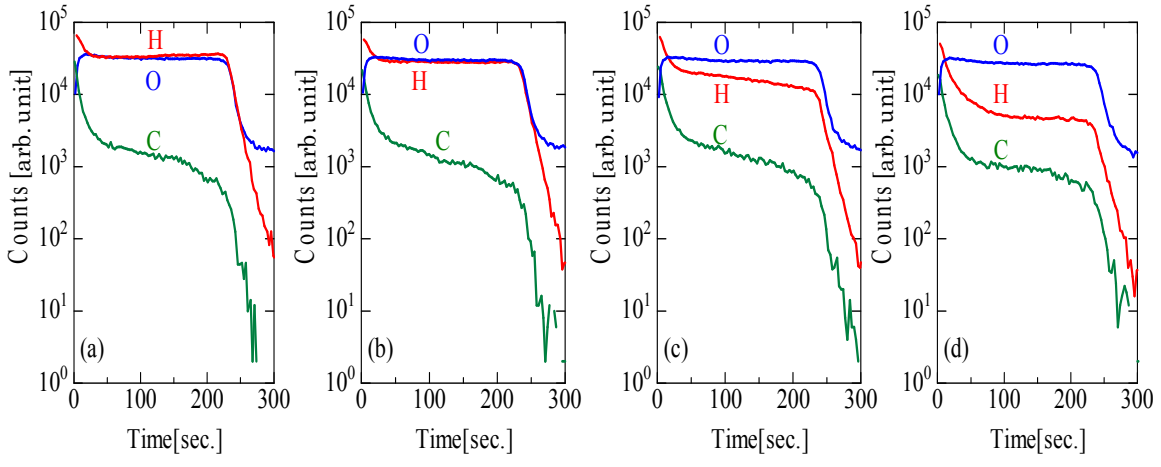

Fig. 7. SIMS profiles of H, O, and C in ZnO films (a) non-annealed, (b) annealed at 200°C, (c) annealed at 300°C, (d) annealed at 400°C, in O2 ambient.

temperature. In the samples annealed at 300 ℃ and 400 ℃, the reduction of hydrogen was observed as compared with the non-annealed sample as shown in fig. 8. It is considered that the residual hydrogen was released by the annealing. These results suggest that the hydrogen plays an important role for the improvement of reliability.

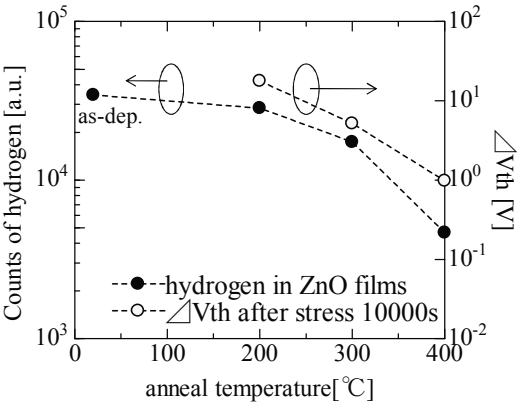

Fig. 8. Dependence of hydrogen in ZnO films and ΔV_{th} on annealing temperature

Based on the results obtained in this study, features of the degradation observed in these TFTs were the marked ΔV_{th} with no ΔS and the recovery properties. As we pointed earlier, such degradation markedly improved and a marked decrease in hydrogen was confirmed in the 400 °C-annealed TFTs. Therefore, residual hydrogen in the ZnO films is possible to accelerate the degradation caused by the electrical stresses.

Summary

We investigated TFTs with ZnO channel layers deposited by PA-ALD at low temperatures. The fabricated ZnO TFTs were annealed at various temperatures in O_2 ambient, and the changes in their electrical properties were measured. ZnO TFTs with post-thermal annealing in O_2 ambient stably exhibited clear transistor operations with no V_{th} shift or degradation in *S.S.* regardless of annealing temperature. In addition, the (002) peak of the films had a slightly larger intensity than the (100) peak, and a shift of the (002) peak was observed for the films annealed above 300 ℃. These results suggest that the improvements in the transfer characteristics of ZnO TFTs are attributed to the change of the crystallinity of these TFTs.

Furthermore, the ZnO TFTs annealed at 400 ℃ showed low V_{th} shift with bias stress. SIMS analysis revealed a marked reduction in hydrogen by the annealing at 400 ℃. Hydrogen is introduced during the deposition of a film. Therefore, the control of hydrogen concentration will be the key issue in promoting the reliability. Through this study, we found that electrical properties of ZnO TFTs are dependent on the annealing temperature, and the threshold voltage shifts by the stress seem to be caused by the residual hydrogen in ZnO films.

Acknowledgments

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