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Thin-Film Transistor Fabricated on the $SrTiO_3$ Epitaxial Film Annealed in an Oxygen Atmosphere

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Abstract. We report herein fabrication and characterization of a thin-film transistor (TFT) using a $SrTiO_3$ epitaxial film grown on (001) face of LSAT $[(LaAlO_3)_{0.3}(Sr_2AlTaO_6)_{0.7}]$ substrate by a pulsed laser deposition technique. Abrupt stepped-and-terraced surface of $SrTiO_3$ film, which can be obtained by the thermal annealing of the layer-by-layer grown $SrTiO_3$ film at 900ºC in an oxygen pressure of ~1 Pa, is found to be a key material to obtain excellent TFT characteristics. In the present case, the $SrTiO_3$-TFT exhibits following characteristics at room temperature: on-to-off current ratio $>10^5$, threshold gate voltage V_{th} = +6.5 V, sub-threshold swing S-factor ~2.1 Vdecade^{-1}, and field effect mobility μ_{FE} ~0.8 cm^{2}V^{-1}s^{-1}.

Introduction

Strontium titanate ($SrTiO_3$, cubic perovskite, *Pm*3*m*, lattice constant a =3.905 Å) is known as a band insulator with a wide bandgap of ~3.2 eV. $SrTiO_3$ has attracted growing attention for the next generation of oxide electronics because $SrTiO_3$ exhibits several unique properties: Charge carrier concentration of $SrTiO_3$ can be easily controlled from insulator to metal (n_{3D} ~10^{21} cm^{-3}) by appropriate substitutional doping such as Nb or La [1,2]. $SrTiO_3$ exhibits extremely high Hall mobility of $>10^4$ cm^{2}V^{-1}s^{-1} at 2 K [3]. High quality single crystals of $SrTiO_3$, which is commercially available, are widely applied for the heteroepitaxial film growth of several perovskite oxides. Recent finding of high-density two-dimensional electron gas (2DEG) by Ohtomo and Hwang [4], which is confined within extremely thin layer at the

$LaAlO_3/SrTiO_3$ heterointerface, accelerates the motivation toward the realization of $SrTiO_3$-based electronic devices.

In order to realize the $SrTiO_3$-based electronic devices, $SrTiO_3$-based field effect transistor (FET) is essentially important because charge carrier density in $SrTiO_3$ can be modulated electrostatically. A number of $SrTiO_3$-based FETs have been reported to date using high quality single crystals of $SrTiO_3$ with stepped and terraced surface [5-10]. Very recently, Ueno and co-workers observed superconducting transition (T_c ~0.4 K) of electrostatically accumulated two-dimensional electron channel (sheet charge concentration, n_{2D} =1−10 × 10^{13} cm^{-2}) in $SrTiO_3$ single crystal using electric double layer gating technique [11]. They modulated the mean depth of carrier distribution from 16 to 3 nm, which is far thinner than the thickness of single crystal plate (~100 μm). Thus, one considers that $SrTiO_3$-based thin film transistor (TFT) with good transistor characteristics is appropriate to further clarify the condensed-matter physics of $SrTiO_3$. However, $SrTiO_3$-based thin TFT has not been reported so far.

In our preliminary study, we fabricated $SrTiO_3$-TFTs using as-deposited $SrTiO_3$ epitaxial films, which were composed of several grains. The resultant TFT was normally-on type transistor and the values of the on−to−off current ratio and S-factor are <10^2 and ~20 $Vdecade^{-1}$, indicating that oxygen vacancies and/or carrier traps were generated in the $SrTiO_3$ film (data not shown). In order to improve the TFT characteristics, the as-deposited $SrTiO_3$ films were annealed in an oxygen atmosphere.

Here we report fabrication and characterization of $SrTiO_3$ TFTs using high quality epitaxial films of $SrTiO_3$, which was obtained by the thermal annealing of the layer-by-layer grown $SrTiO_3$ film at 900ºC in an oxygen pressure ~1 Pa. We selected amorphous $12CaO{\cdot}7Al_2O_3$ (*a*-C12A7, permittivity ε_r = 12) as the gate insulator for the fabrication of TFT because *a*-C12A7 gated $SrTiO_3$ FETs exhibit excellent transistor characteristics [10]. The resultant $SrTiO_3$-TFT exhibits following characteristics at room temperature: on-to-off current ratio >10^5, sub-threshold swing ~2.1 $Vdecade^{-1}$, and field effect mobility ~0.8 $cm^2V^{-1}s^{-1}$.

Experimental

$SrTiO_3$ epitaxial films (thickness: ~60 nm) were fabricated on (001) face of LSAT [$(LaAlO_3)_{0.3}(Sr_2AlTaO_6)_{0.7}$] substrates by a pulsed laser deposition (PLD) technique (KrF excimer laser, ~0.5 $Jcm^{-1}pulse^{-1}$, 20 ns, 5 Hz). During the film deposition, we monitored specular spot intensity of reflection high energy electron diffraction (RHEED) to control the film thickness. Substrate temperature was kept at 900ºC during the film deposition. After the film deposition, pure O_2 gas was additionally introduced into the PLD chamber to fill up oxygen deficiency of the $SrTiO_3$ film. Then, the film was cooled down to room temperature. Crystallographic orientation and thickness of the films were evaluated by high resolution x-ray diffraction (HRXRD, ATX-G, Rigaku Co.) using monochrometed Cu $K\alpha_1$ beam.

Then, we fabricated a top-gate-type TFT structure on the $SrTiO_3$ single crystal films as schematically shown in Fig. 1. First, 20-nm-thick metallic Ti films, used as the source and drain electrodes, were deposited through a stencil mask by electron beam (EB) evaporation (base pressure ~10^{-4} Pa, no substrate heating). Then, 160 nm-thick amorphous-$12CaO \cdot 7Al_2O_3$ (*a*-C12A7, ε_r=12) film was deposited through a stencil mask by PLD (~3 $Jcm^{-2}pulse^{-1}$, oxygen pressure ~0.1 Pa) using dense polycrystalline C12A7 ceramic as target. Finally, gate electrode, which is 20-nm-thick metallic Ti film, was deposited through a stencil mask by EB evaporation. The resultant TFTs were annealed at 200ºC in air atmosphere to reduce off current.

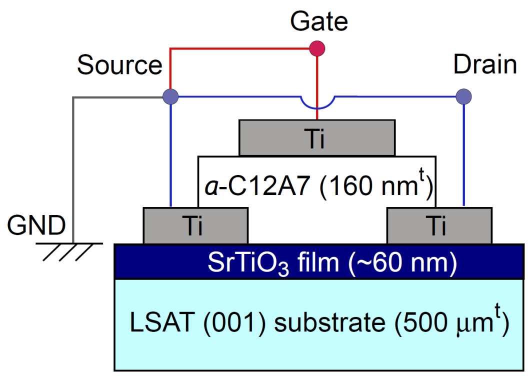

Fig. 1: Schematic structure of the $SrTiO_3$-TFT. Ti films (20 nm thick) are used as the source, drain and gate electrodes. A 160 nm-thick *a*-C12A7 film is used as the gate insulator. Channel length (*L*) and channel width (*W*) are 200 and 400 μm, respectively.

Results

In the out of plane XRD pattern of the resultant $SrTiO_3$ film, Pendellösung fringes were clearly observed at around 002 diffraction peak of $SrTiO_3$ (data not shown). Thus, we confirmed the film thickness (60 nm) using the Pendellösung fringes. Surface morphology was observed by an atomic force microscope (AFM, NanoScope E, D.I.)[Fig. 2(a)]. Stepped and

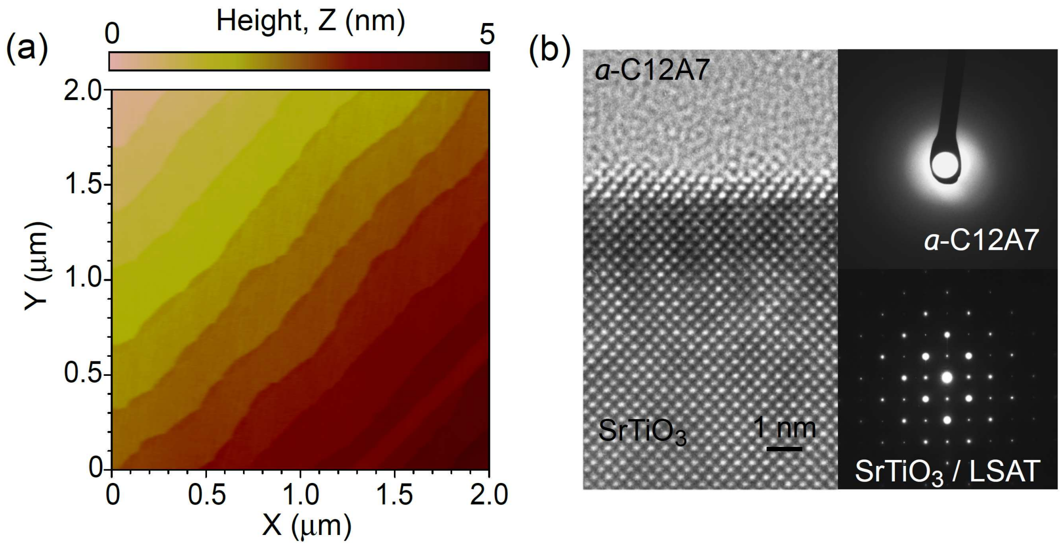

Fig. 2: (a)Topographic AFM image of the $SrTiO_3$ epitaxial film annealed in an oxygen atmosphere [Oxygen pressure: 1 Pa]. (b)Cross-sectional high-resolution transmission electron microscope (HRTEM) images of the 160-nm-thick *a*-C12A7/$SrTiO_3$/LSAT heterointerface.

terraced surface are seen. Figure 2(b) shows the cross sectional high-resolution transmission electron microscope image of the *a*-C12A7/$SrTiO_3$/LSAT interface region (HRTEM, TOPCON EM-002B, acceleration voltage of 200 kV, TOPCON). Featureless structure of *a*-C12A7 is seen though lattice image is clearly seen in the $SrTiO_3$ film. A broad halo pattern is seen in the selected area electron diffraction patterns o f *a*-C12A7, indicating that *a*-C12A7 glass film was deposited on the $SrTiO_3$ film.

Transistor characteristics of the resultant $SrTiO_3$-TFTs were measured by using a semiconductor device analyzer (B1500A, Agilent Technologies) at room temperature. The channel width (W) and the channel length (L) of the TFT are 400 and 200 µm, respectively. Figure 3 shows typical (a) transfer and (b) output characteristics of the resultant TFT. Drain current (I_d) of the FET increased as the gate voltage (V_g) increased, hence the channel was *n*-type, and electron carriers were accumulated by positive V_g [Fig. 3(a)]. Rather large threshold gate voltage (V_{gth}) of +6.5 V, obtained from a linear fit of an $I_d^{0.5}$-V_g plot [inset of (a)], is observed, which corresponds electron trapping state density of ~5 × 10^{12} cm^{-2}. We observed a clear pinch-off and current saturation in I_d [Fig. 3(b)], indicating that the operation of this FET conformed to standard FET theory. The on—to—off current ratio, S-factor and threshold voltage, are >10^5, ~2.1 $Vdecade^{-1}$ and +6.5 V, respectively. We then calculated the sheet charge concentration (n_{xx}), and the field effect mobility (μ_{FE}) of the $SrTiO_3$-TFTs. The n_{xx} values were obtained from $n_{xx} = C_i\,(V_g - V_{th})$, where C_i was the capacitance per unit area (67 $nFcm^{-2}$). The μ_{FE} values were obtained from $\mu_{FE} = g_m[(W/L)C_i \cdot V_d]^{-1}$, where g_m is transconductance $\partial I_d/\partial V_g$. The maximum μ_{FE} of the TFT was ~0.8 $cm^2V^{-1}s^{-1}$ (V_g = 47 V, n_{xx} = 2.0 × 10^{13} cm^{-2}).

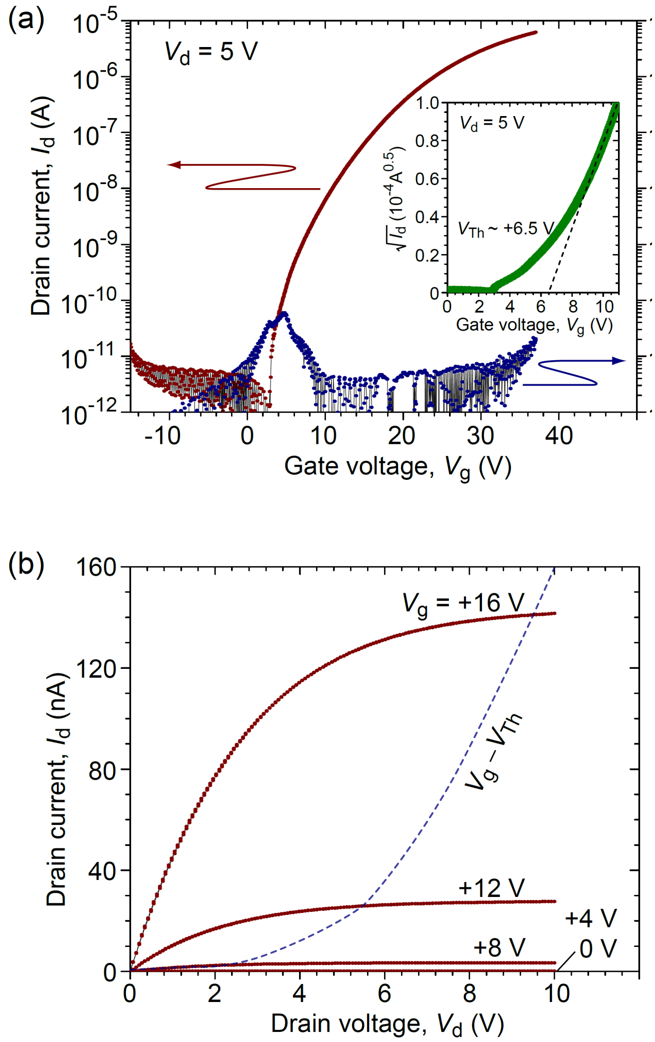

Fig. 3. (a) Typical transfer and (b) output characteristics of the TFT using the high quality $SrTiO_3$ epitaxial film, which was annealed in an oxygen atmosphere. The inset of (a) shows $I_d^{0.5}$-V_g plot of the TFT.

Summary

We have demonstrated fabrication and device characteristics of a thin-film transistor (TFT) fabricated in single-crystalline $SrTiO_3$ thin film grown on (001) face of $(LaAlO_3)_{0.3}(Sr_2AlTaO_6)_{0.7}$ substrate by a pulsed laser deposition technique. Abrupt stepped-and-terraced surface of $SrTiO_3$ film, which can be obtained by the thermal annealing of the layer-by-layer grown $SrTiO_3$ film at 900ºC in an oxygen pressure of ~1 Pa, is found to be a key material to obtain excellent TFT characteristics. In the present case, the $SrTiO_3$-TFT exhibits following characteristics at room temperature: on-to-off current ratio $>10^5$, sub-threshold swing ~2.1 $Vdecade^{-1}$, and field effect mobility ~0.8 $cm^2V^{-1}s^{-1}$.

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