Characteristic Evaluation of Complementary Inverter using Amorphous Oxide TFT and Polymer Organic TFT

Takashi Nakanishi[1], Mariko Sakemi[1], Tomoya Okumura[1], Yuki Ueda[1], Mutsumi Kimura[1], Kenji Nomura[2], Toshio Kamiya[2], Hideo Hosono[2] and Takashi Aoki[3]

[1] Ryukoku University, Seta, Otsu, 520-2194, Japan, mutsu@rins.ryukoku.ac.jp
[2] Tokyo Institute of Technology, Nagatsuta, Midori, Yokohama 226-8503, Japan
[3] Seiko Epson Corporation, Fujimi, Nagano, 399-0293, Japan

Keywords: Complementary Inverter, Amorphous Oxide TFT, Polymer Organic TFT

Abstract. A complementary inverter is composed by combining an amorphous oxide TFT and polymer organic TFT, and its characteristic is evaluated. It is found that the complementary inverter correctly works in DC operation with a proper gain. However, the input-output characteristic gradually delays at a high sweep rate in transient operation due to the insufficient performance of the polymer organic TFT and large load capacitance. It is concluded that the design parameters such as transistor performances, gate-drain capacitances, load capacitance and operation frequency should be optimized in order to produce the actual circuit.

Introduction

Recently, oxide TFTs are promising for various applications from flat-panel displays (FPDs) such as liquid-crystal displays (LCDs), organic light-emitting diode displays (OLEDs) and

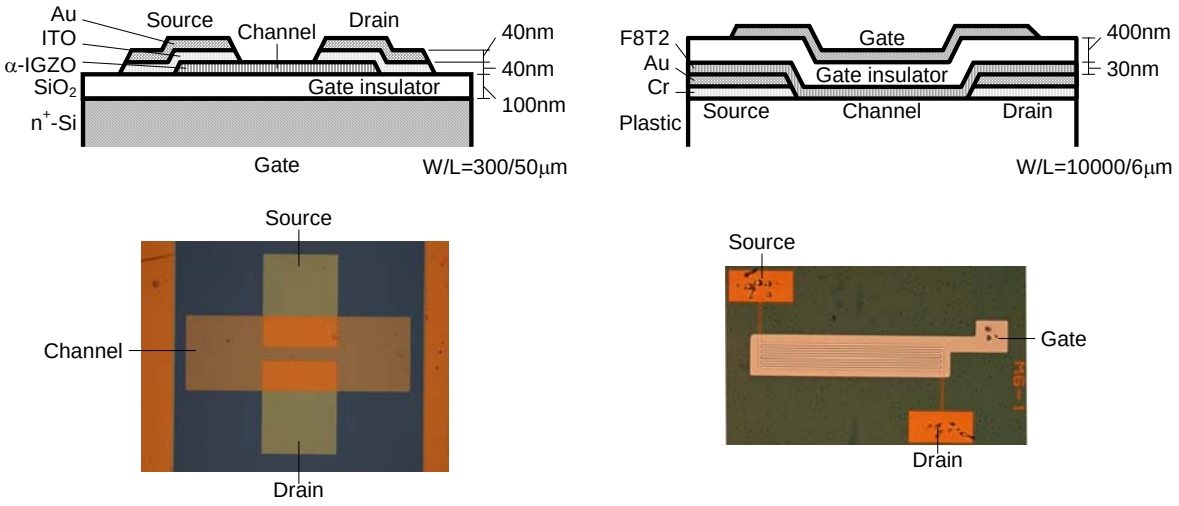


Fig. 1
Device structures of the amorphous oxide TFT and polymer organic TFT.

electronic papers to electronics components because they are transparent and can be fabricated on flexible substrates at low temperature [1-2]. In particular, since amorphous oxide TFTs can be fabricated on plastic substrates at room temperature using low-temperature processes such as sputtering and pulsed laser deposition (PLD) and have high and uniform performances, they have been extensively studied [3-4]. However, n-type TFTs have been mainly reported for the amorphous oxide TFTs, and p-type TFTs with sufficient performance and reliability have been hardly reported [5].

On the other hand, organic TFTs are also promising because they can be fabricated on flexible substrates at low temperature [6]. In particular, since polymer organic TFTs can be fabricated on plastic substrates at room temperature with low cost using printing technologies such as spin coating, offset printing, screen printing and ink jetting, they have been also extensively studied [7-9]. However, p-type TFTs have been mainly reported for the polymer organic TFTs, and n-type TFTs with sufficient performance and reliability have been hardly reported [10].

To date, we have analyzed various TFTs such as poly-Si TFTs, amorphous Si TFTs, polycrystalline oxide TFTs, amorphous oxide TFTs and polymer organic TFTs. Among these TFTs, prospective candidates for n-type TFTs are amorphous oxide TFTs while prospective candidates for p-type TFTs are polymer organic TFT because both TFTs can be fabricated on plastic substrates at room temperature. In this paper, a complementary inverter is composed by combining an amorphous oxide TFT and polymer organic TFT, and its characteristic is evaluated. Although the complementary inverter using a polycrystalline oxide TFT and low-molecule organic TFT was reported [11], the complementary inverter using an amorphous oxide TFT and polymer organic TFT is more attractive because of the reason written above [12].

Device structure and fabrication process

The device structure of the amorphous oxide TFT is shown in Fig. 1. The bottom-gate and top-contact TFT is fabricated as follows. First, a heavily-doped n^+-Si substrate is used as the gate terminal, and a thermally oxidized SiO_2 film is used as the gate insulator. After the necessary areas are patterned by photolithography of photoresist, an amorphous $InGaZnO_4$ (α-IGZO) film is deposited by PLD at room temperature in oxygen gas at 6.2 Pa, patterned by lift-off technique and used as the channel layer. After the necessary areas are patterned by photolithography, an indium-tin-oxide (ITO) film and Au film are sequentially deposited by PLD, patterned by lift-off technique and used as the source and drain terminals.

The device structure of the polymer organic TFT is also shown in Fig. 1. The top-gate and bottom-contact TFT is fabricated as follows. First, a plastic substrate is used. Next, a Cr film and Au film are sequentially deposited,

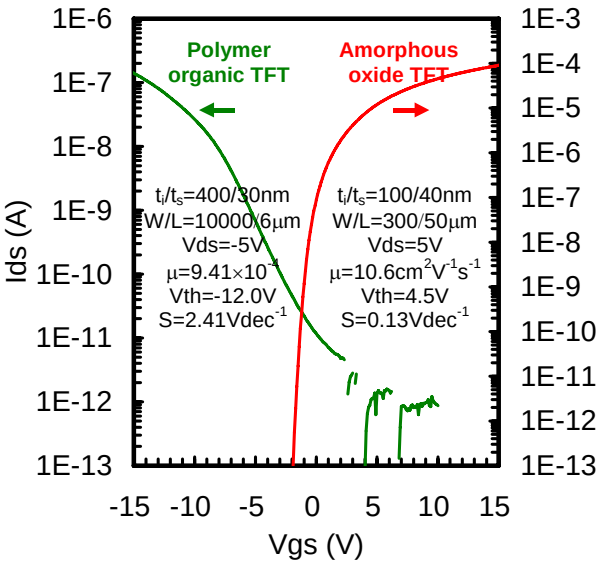


Fig. 2
Transistor characteristics of the amorphous oxide TFT and polymer organic TFT.

patterned by photolithography and etching and used as the source and drain terminals. Next, an F8T2 film is deposited by spin coating and drying and used as the channel layer, and an insulator film is also deposited by spin coating and drying and used as the gate insulator. Finally, a metal film is deposited by mask evaporation and used as the gate terminal.

Since both TFTs are fabricated at room temperature as written above, although each TFT are fabricated on each substrate here, it is possible in principle to be fabricated and integrated on a plastic substrate. Moreover, it is also possible to be formed in a 3-D stacked structure with the amorphous oxide TFT under the polymer organic TFT or vice versa.

Transistor characteristic

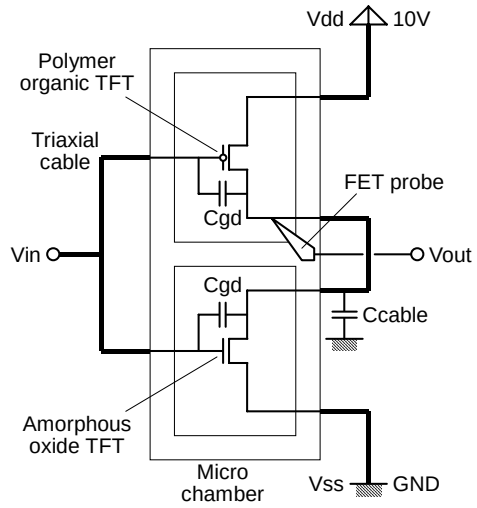
The transistor characteristic of the amorphous oxide TFT is shown in Fig. 2. The thickness of the gate insulator (t_i) is 100 nm, the thickness of the channel layer (t_s) is 40 nm, the gate width (W) / gate length (L) is 300 / 50 μm, the gate voltage (Vgs) is -10 ~ 15 V, and the drain voltage (Vds) is 5 V. The field-effect mobility (μ) is 10.6 $cm^2V^{-1}s^{-1}$, the threshold voltage (Vth) is 4.5 V, and the sub-threshold swing (S) is 0.13 $Vdec^{-1}$.

The transistor characteristic of the polymer organic TFT is also shown in Fig. 2. t_i = 400 nm, t_s = 30 nm, W / L = 10000 / 6 μm, Vgs = 10 ~ -15 V, and Vds = -5 V. μ = 9.41×10^{-4} $cm^2V^{-1}s^{-1}$, Vth = -12.0 V, and S = 2.41 $Vdec^{-1}$.

The necessary condition for complementary circuits in consideration of the higher supplied voltage (Vdd) and lower supplied voltage (Vss) is that the on current of the n-type TFT at Vgs = Vdd - Vss is larger than the off current of the p-type TFT at Vgs = 0, and the on current of the p-type TFT at Vgs = - (Vdd - Vss) is larger than the off current of the n-type TFT at Vgs = 0. This necessary condition can be satisfied by Vdd = 10 V and Vss = GND in spite of the insufficient performance of the polymer organic TFT. Therefore, these Vdd and Vss are used below, and it is expected that the complementary inverter correctly works.

Inverter characteristic

The complementary inverter using the amorphous oxide TFT and polymer organic TFT is shown in Fig. 3. The amorphous oxide TFT is used as the n-type TFT while the polymer organic TFT is used as the p-type TFT, and they are located in the micro chamber and connected by the triaxial cables outside the micro chamber. The load capacitance of the complementary inverter (Cload) consists of the gate-drain capacitances (Cgd) of the amorphous oxide



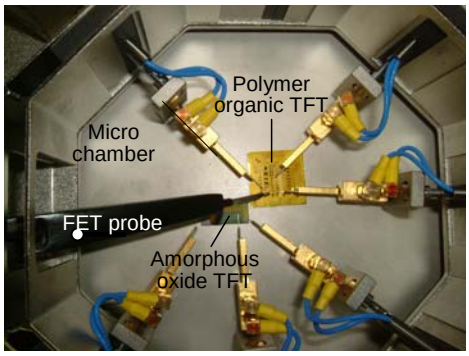


Fig. 3
Complementary inverter using the amorphous oxide TFT and polymer organic TFT.

TFT and polymer organic TFT and the wiring capacitance of the triaxial cables and is no less than the order of 1 nF. Vdd = 10 V, Vss = GND, the input voltage (Vin) is -10 ~ 10 V in the DC operation, and the sweep rate of the triangle wave of Vin is 20 ~ 2k Vs^{-1} in the transient operation. The output voltage is measured using the FET probe with excellently low input capacitance and leakage current. Although Vin should be Vss ~ Vdd in general, since the transistor characteristic of the amorphous oxide TFT is unwillingly shifted to depletion side and the transistor characteristic of the polymer organic TFT is unwillingly shifted to enhancement side, Vin is reluctantly set to be lower than Vss. However, the following conclusion will be reasonable in general.

The input-output characteristic of the complementary inverter using the amorphous oxide TFT and polymer organic TFT in the DC operation is shown in Fig. 4. It is found that the complementary inverter correctly works in DC operation with a proper gain. The inversion voltage is about 2 V, and the gain is about 80.

The input-output characteristic of the complementary inverter using the amorphous oxide TFT and polymer organic TFT in the transient operation is shown in Fig. 5. The input-output characteristic does not delays very much for Vin > 2 V and translation from the higher Vout to the lower Vout. This is due to the sufficient performance of the amorphous oxide TFT. On the other hand, the input-output characteristic gradually delays at a high sweep rate in transient operation for Vin < 2 V and translation from the lower Vout to the higher Vout. This is due to the insufficient performance of the polymer organic TFT and large Cload. Moreover, the direct capacitance coupling also affects the input-output characteristic due to the large Cgd. As a result, it is concluded that the design parameters such as transistor performances, Cgd, Cload and operation frequency should be optimized in order to produce the actual circuit.

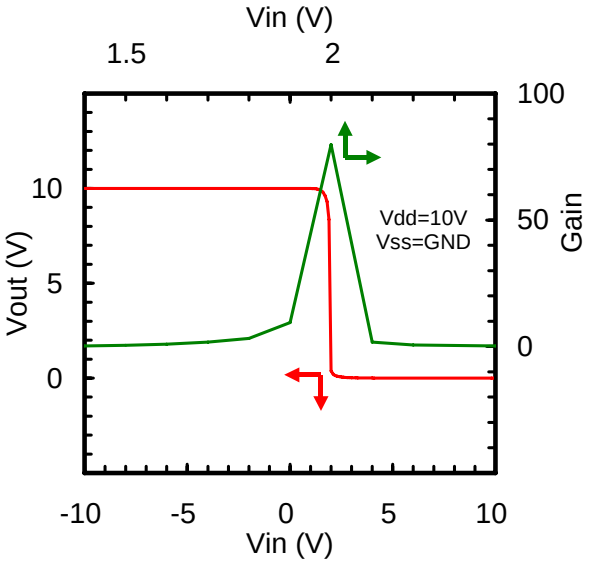


Fig. 4
Input-output characteristic of the complementary inverter using the amorphous oxide TFT and polymer organic TFT in the DC operation.

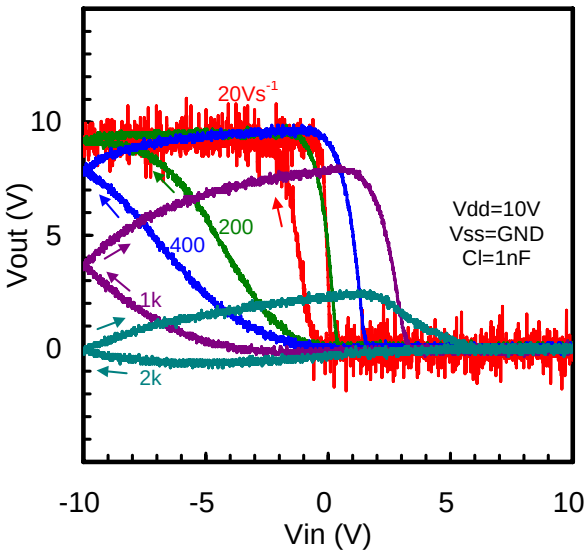


Fig. 5
Input-output characteristic of the complementary inverter using the amorphous oxide TFT and polymer organic TFT in the transient operation.

Conclusion

A complementary inverter was composed by combining an amorphous oxide TFT and polymer organic TFT, and its characteristic was evaluated. It was found that the complementary inverter correctly works in DC operation with a proper gain. However, the input-output characteristic gradually delays at a high sweep rate in transient operation due to the insufficient performance of the polymer organic TFT and large Cload. It was concluded that the design parameters such as transistor performances, Cgd, Cload and operation frequency should be optimized in order to produce the actual circuit.

Acknowledgments

The authors wish to thank Dr. Junichi Karasawa, Dr. Soichi Moriya, Dr. Tsutomu Miyamoto, Dr. Takeo Kawase, Dr. Hideyuki Kawai and Dr. Satoshi Inoue of Seiko Epson Corporation. This research is partially supported by a grant for Industrial Technology Research from the New Energy and Industrial Technology Development Organization (NEDO), collaborative research with Seiko Epson, a research project of the Joint Research Center for Science and Technology at Ryukoku University, a grant from the High-Tech Research Center Program (HRC) for private universities from the Ministry of Education, Culture, Sports, Science and Technology (MEXT), a grant for research facility equipment for private universities from MEXT, and a grant for special research facilities from the Faculty of Science and Technology of Ryukoku University.

References

[1] K. Nomura, H. Ohta, K. Ueda, T. Kamiya, M. Hirano and H. Hosono, Science 300, 1269 (2003).
[2] T. Hirao, M. Furuta, H. Furuta, T. Matsuda, T. Hiramatsu, H. Hokari, M. Yoshida, H. Ishii and M. Kakegawa, J. SID 15, 17 (2007).
[3] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano and H. Hosono, Nature 432, 488 (2004).
[4] M. Kimura, T. Nakanishi, K. Nomura, T. Kamiya and H. Hosono, Appl. Phys. Lett. 92, 133512 (2008).
[5] Y. Ogo, H. Hiramatsu, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano and H. Hosono, Appl. Phys. Lett. 93, 032113 (2008).
[6] M. Nakamura, AM-FPD '08, 105
[7] H. Sirringhaus, T. Kawase, R. H. Friend, T. Shimoda, M. Inbasekaran, W. Wu and E. P. Woo, Science 290, 2123 (2000).
[8] T. Okumura, Y. Ueda, M. Kimura, J. Karasawa, T. Aoki and S. Moriya, The 4th Thin Film Materials and Devices Meeting, 204 (2007).
[9] T. Aoki, S. Moriya, T. Miyamoto, H. Kawai, T. Okumura, Y. Ueda and M. Kimura, The 4th Thin Film Materials and Devices Meeting (2007).
[10] L.-L. Chua, J. Zaumseil, J.-F. Chang, E. C.-W. Ou, P. K.-H. Ho, H. Sirringhaus, R. H. Friend, Nature 434, 194 (2005).
[11] M. S. Oh, D. K. Hwang, K. Lee, S. Im and S. Yi, Appl. Phys. Lett. 90, 173511 (2007).
[12] T. Nakanishi, M. Sakemi, T. Okumura, Y. Ueda, M. Kimura, K. Nomura, T. Kamiya, H. Hosono and T. Aoki, The 5th Thin Film Materials and Devices Meeting, 176 (2008).